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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,305	12/16/2003	Kassem M. Abdallah	EMC-03-104	5962

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,305	ABDALLAH ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,13-17,25 and 28-31* is/are rejected.

7)☒ Claim(s) *5-12,18-24,26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 13-17, 25, and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Derrick et al.

As broadly drafted, these claims do not define any structure/step that differs from Derrick et al. (Derrick, 5,782,980).

With regard to claim 1, Derrick discloses a system for arbitrating access to a shared resource (shown generally at Fig. 4) comprising:

a plurality of microprocessors (406, see also col. 1, lines 22-27 and 31-43); a shared resource (408, Fig. 4 or 706, Fig. 7); and a controller (402, Fig. 4 or 710, Fig. 7) coupled to the plurality of microprocessors (406, see also col. 1, lines 22-27 and 31-43) and the shared resource (408, Fig. 4 or 706, Fig. 7) by a first bus (bus 404 connecting

the bus masters to the bus controller 402; or local bus 704, Fig. 7) and a second bus (the bus connecting the shared resource to the bus controller as shown in Fig. 4 or the bus connecting the system memory 706 to the controller 710 as shown in Fig. 7), respectively, the controller (402, Fig. 4 or 710, Fig. 7) including a register (spin buffer 502 of the controller 710, for example, includes at least one register 520) having a lock portion associated with each of the plurality of processors (ID field associated with each of the plurality of masters/processors, see at least col. 5, lines 2-51) and at least one status portion (field containing 1 bit LOCK, see at least col. 5, lines 2-51), each of the lock portions (ID field associated with each of the plurality of masters/processors) indicating whether the associated one of the plurality of microprocessors has obtained access to communicate with the shared resource (see at least col. 5, line 2 to col. 6, line 53) and each of the at least one status portions (field containing 1 bit LOCK) includes a bit indicating whether any of the plurality of microprocessors has obtained access to communicate with the shared resource (see at least col. 5, line 2 to col. 6, line 53).

With regard to claim 2, it is clear that the shared resource comprises a memory device such as memory 706.

With regard to claim 3, it is clear that the system of Derrick includes includes a plurality of shared resources (see at least Fig. 4).

With regard to claim 4, it is clear that the register includes at least as many lock portions and status portions as there are shared resources, wherein each shared resource has a lock portion and a status portion associated therewith (see at least Fig. 5 and description thereof; see also col. 5, line 2 to col. 6, line 53).

With regard to claim 13, Derrick discloses a controller (shown generally at Figs. 4-7) for arbitrating access to at least one shared resource (408/706) by a plurality of processors (406, see also col. 1, lines 22-27 and 31-43), the controller comprising: a first register portion (registers used for "ID" included in spin buffer 502, Fig. 5, for example) including a plurality of layers (a plurality of stacked registers), each of the plurality of layers being associated with a different one of the plurality of processors (406, see also col. 1, lines 22-27 and 31-43), each of the plurality of layers (a plurality of registers 520) including an access indication portion (ID filed, see at least col. 5, lines 2-51) associated with each of the at least one shared resource (408/706), the access indication portion (ID filed, see at least col. 5, lines 2-51) holding an indicator (M bits) of whether a processor (406, see also col. 1, lines 22-27 and 31-43) associated with a particular layer (a plurality of registers) has obtained access to communicate with the shared resource associated with the access indication portion of the particular layer (see at least col. 5, lines 2-51); and an access arbitration device (arbiter 506, Fig. 5/arbitration logic, Fig. 4), for example) associated with all of the access indication portions (of spin buffer 502 associated with arbiter 506, Fig. 5/arbitration logic, Fig. 4) of each of the at least one shared resources (408/706) for controlling access to the associated shared resource (408/706) by the plurality of processors (406, see also col. 1, lines 22-27 and 31-43), the access arbitration device (arbiter 506, Fig. 5/arbitration logic, Fig. 4, for example) including an input for receiving access indication signals from the plurality of processors (it is clear that the so-called "access indication signals" from the masters/processors must be received by the arbiter before arbitration can be

performed), the access arbitration device: (A) determining whether the at least one shared resource is being accessed by any of the plurality of processors (the arbiter must first determine whether the shared resource is free before granting access to one of the masters/processors); and (B) arbitrating access to the shared resource based on the determination made Step (A) (it is clear that if the shared resource is determined to be free then arbitration can be performed by the arbiter employing an arbitration logic).

With regard to claim 14, in Derrick, if a particular processor of the plurality of processors ((406, see also col. 1, lines 22-27 and 31-43) requires access to a particular one of the at least one shared resources (408/706), it inputs an access indicator to the input of the access arbitration device associated with the particular shared resource and, no other processor has access to the shared resource, as determined in Step (A) (the arbiter must first determine whether the shared resource is free before granting access to one of the masters/processors), the access arbitration device grants access to the particular shared resource by the particular processor (it is clear that if the shared resource is determined to be free then arbitration can be performed by the arbiter employing an arbitration logic).

With regard to claim 15, in Derrick, if a particular processor of the plurality of processors requires access to a particular one the at least one shared resources, it inputs an access indicator to the input of the access arbitration device associated with the particular shared resource and, if another processor has access to the shared resource, as determined in Step (A), the access arbitration device denies access to the

particular shared resource by the particular processor (it is clear that if a shared resource is accessed by a particular master/processor, then the arbiter denies access to the shared resource; arbitration among masters/processors is performed only when the shared resource is free or available for accessing).

With regard to claim 16, in Derrick, the access arbitration device grants access to the particular shared resource by the particular processor by passing the access indicator input to the access arbitration device by the particular processor to the access indication portion for the particular shared resource in the layer associated with the particular processor (if a particular master/processor gains access to the shared resource via arbitration, the LOCK bit is set in the registers of the spin buffer).

With regard to claim 17, in Derrick, it is clear that the access arbitration device denies access to the particular shared resource by the particular processor by clearing the access indicator input to the access arbitration device by the particular processor (when the shared resource is not available, the request for access to the shared resource of a particular master/processors is denied, and according to the principle of arbitration, the master/processor must retry, or in other words, the access indicator input to the access arbitration device by the particular processor is cleared by a new access indicator input to the access arbitration device by the particular processor must provided to the arbiter for arbitration for access to the shared resource.

With regard to claim 25, the controller of Derrick further comprises a second register portion (registers for "LOCK" included in spin buffer 502) including a status indication portion (LOCK bit) associated with each of the at least one shared resources,

each status indication portion including a status indicator which indicates whether the shared resource associated with the status indication portion is being accessed by one of the plurality of processors (see at least col. 5, lines 2-51).

With regard to claims 28-31, see discussion above and further discussion below in response to Applicants' remarks and arguments.

Response to Arguments

Applicants' arguments filed 3/24/2006 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 35 USC 112 Rejection:

The amendment to claim 28, filed 3/24/2006, overcomes the 35 USC 112, 2nd paragraph rejection.

The Derrick 102 Rejection:

With regard to claim 1, Applicants argue that "the system of the present invention includes, among other features, a register having a lock portion associated with each of the plurality of processors. To the contrary, the device of Derrick has a register associated with each of the semaphores/resources. Derrick does not teach or suggest a lock portion associated with each of a plurality of processors. In fact, Derrick only teaches a memory location in the register in which a lock bit is written if a device takes ownership of the semaphore/resource associated with the particular register assigned to the semaphore. While the examiner states that Derrick teaches ID fields associated with each processor, this is not the case. As stated above, each register 520 includes an ID field for the identification of the master that currently owns the associated resource. However, when that master no longer owns that resource, and a different master takes ownership, that ID field then includes the identification of the new master. Therefore, the ID field in each register is not associated with each processor, as the information in that field can identify any of the masters that take ownership of the resource associated with the register."

Contrary to Applicants' argument, Derrick clearly discloses that "[v]arious methods may be employed to encode the ID and lock information within memory locations 520A-520Z, as shown in more detail in FIGS. 8-10. Referring to FIG. 8, a first method of encoding the lock and ID information uses a single lock bit, and a number M of bits sufficient to binarily encode each device that needs to access the shared resource with a unique ID. Thus, if there are eight devices in a system, three bits in the ID field would be required, with each of the eight binary combination corresponding to one of the devices. With this type of encoding scheme, the LOCK bit is set if the shared resource corresponding to the spin buffer location is owned by another device, and the binary encoding in the ID field indicates which device owns the shared resource. " See Derrick, column 5, lines 9-22. Thus, it is clear that each ID field in the memory location (register) is associated with each of a plurality of processors, and a single lock bit indicates whether any of the processors has obtained access to the shared resource. Further, Derrick discloses that "an alternative scheme is known as 'one hot' encoding. In this scheme, a separate lock bit is provided for each different device, and one of the lock bits are set if the corresponding device owns the shared resource. Referring to FIG. 10, yet another encoding scheme has a single lock bit, with a separate ID bit corresponding to each device that must share the shared resource." See Derrick, column 5, lines 22-33. Thus, it is clear that each ID field in the memory location (register) is associated with each of a plurality of processors, and the lock bit(s) indicates whether any of the processors has obtained access to the shared resource.

With regard to claim 13, Applicants argue that "Derrick does not teach a first register portion including a plurality of layers, each of the plurality of layers being associated with a different one of the plurality of processors. There is no disclosure in Derrick that teaches or suggests that any part of the spin buffer 502, which includes registers 520, is associated with a different one of the masters that seek ownership of the semaphores. In Derrick's system, each register 520 is associated with a different semaphore, but no registers are associated with a different master. Furthermore, Derrick does not teach or suggest an access indication portion which holds an indicator of whether a processor associated with a particular layer has obtained access to communicate with the shared resource associated with the access indication portion of the particular layer. The examiner states that the access indication portion of Derrick is the ID field, however, as discussed above, the ID field is a part of the register which is associated with a semaphore."

Contrary to Applicants' argument, Derrick discloses a controller (shown generally at Figs. 4-7) for arbitrating access to at least one shared resource (408/706) by a plurality of processors (406, see also col. 1, lines 22-27 and 31-43), the controller comprising: a first register portion (registers used for "ID" included in spin buffer 502, Fig. 5, for example) including a plurality of layers (a plurality of stacked registers), each of the plurality of layers being associated with a different one of the plurality of processors. Further, Derrick clearly discloses that "[v]arious methods may be employed to encode the ID and lock information within memory locations 520A-520Z, as shown in more detail in FIGS. 8-10. Referring to FIG. 8, a first method of encoding the lock and

ID information uses a single lock bit, and a number M of bits sufficient to binarily encode each device that needs to access the shared resource with a unique ID. Thus, if there are eight devices in a system, three bits in the ID field would be required, with each of the eight binary combination corresponding to one of the devices. With this type of encoding scheme, the LOCK bit is set if the shared resource corresponding to the spin buffer location is owned by another device, and the binary encoding in the ID field indicates which device owns the shared resource. " See Derrick, column 5, lines 9-22. Thus, it is clear that each ID field in the memory location (register) is associated with each of a plurality of processors, and a single lock bit indicates whether any of the processors has obtained access to the shared resource. Further, Derrick discloses that "an alternative scheme is known as 'one hot' encoding. In this scheme, a separate lock bit is provided for each different device, and one of the lock bits are set if the corresponding device owns the shared resource. Referring to FIG. 10, yet another encoding scheme has a single lock bit, with a separate ID bit corresponding to each device that must share the shared resource." See Derrick, column 5, lines 22-33. Thus, it is clear that each ID field in the memory location (register) is associated with each of a plurality of processors, and the lock bit(s) indicates whether any of the processors has obtained access to the shared resource.

Applicants also argue that "Derrick also does not teach an access arbitration device associated with all of the access indication portions for carrying out the steps recited in the claim. While Derrick does disclose an arbiter 506, as pointed out by the examiner, there is absolutely no description in Derrick of the operation of the arbiter."

Contrary to Applicants' argument, Derrick clearly discloses that a "[b]us controller 402 may control accesses by bus masters 406 to shared resources 408 using any suitable scheme. For example, bus controller 402 may include arbitration logic which determines when to grant access to a shared resource 408 to a bus master 406. Bus controller 402 may thus assign bus masters 406 a priority which determines the order of granting their requests for shared resources 408." Note also that arbitration is a computer terminology referring to a set of rules (a priority scheme, for example) used for determining and allocating a shared machine resource to more than one hosts or masters vying for the same resource when the shared resource is available (not being accessed by any host/master).

With regard to claim 28, Applicants argue that "Derrick does not teach processing access indication signals received from each of a plurality of processors. While individual masters may read a register associated with a semaphore, there is no access indication signal in the Derrick system that is received from the masters and then processed by the system. Since there are no access indication signals in Derrick's system, they cannot be stored. Derrick does not teach performing a logic operation on the processed access indication signals to generate an access arbitration signal. Since, as discussed above, Derrick does not teach access indication signals, he cannot teach performing a logic operation on them, nor can he teach receiving a further access indication signal from a particular one of the plurality of processors. Lastly, since no operation of the arbiter 506 is disclosed by Derrick, Denick does not teach or suggest arbitrating access to the shared

resource by the particular processor based on the state of the access arbitration signal."

Contrary to Applicants' argument, Derrick clearly discloses that "[v]arious methods may be employed to encode the ID and lock information within memory locations 520A-520Z, as shown in more detail in FIGS. 8-10. Referring to FIG. 8, a first method of encoding the lock and ID information uses a single lock bit, and a number M of bits sufficient to binarily encode each device that needs to access the shared resource with a unique ID. Thus, if there are eight devices in a system, three bits in the ID field would be required, with each of the eight binary combination corresponding to one of the devices. With this type of encoding scheme, the LOCK bit is set if the shared resource corresponding to the spin buffer location is owned by another device, and the binary encoding in the ID field indicates which device owns the shared resource. " See Derrick, column 5, lines 9-22. Thus, it is clear that each ID field in the memory location (register) is associated with each of a plurality of processors, and a single lock bit indicates whether any of the processors has obtained access to the shared resource. Further, Derrick discloses that "an alternative scheme is known as 'one hot' encoding. In this scheme, a separate lock bit is provided for each different device, and one of the lock bits are set if the corresponding device owns the shared resource. Referring to FIG. 10, yet another encoding scheme has a single lock bit, with a separate ID bit corresponding to each device that must share the shared resource." See Derrick, column 5, lines 22-33. Thus, it is clear that each ID field in the memory location (register) is associated with each of a plurality of processors, and the lock bit(s) indicates whether any of the processors has obtained access to the shared resource.

Further, Derrick clearly discloses that a "[b]us controller 402 may control accesses by bus masters 406 to shared resources 408 using any suitable scheme. For example, bus controller 402 may include arbitration logic which determines when to grant access to a shared resource 408 to a bus master 406. Bus controller 402 may thus assign bus masters 406 a priority which determines the order of granting their requests for shared resources 408." Note also that arbitration is a computer terminology referring to a set of rules (a priority scheme, for example) used for determining and allocating a shared machine resource to more than one hosts or masters vying for the same resource when the shared resource is available (not being accessed by any host/master).

Allowable Subject Matter

Claims 5-12, 18-24, 26, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Examiner